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TITLE: Image display device, image display method and display drive device, together with electronic equipment using the same

ABPR:
This invention relates to an image display device that samples stabilized pixel data within a sampling period, to display an image with no ghosting. A liquid crystal panel 100 consists of pixels disposed at pixel positions formed at intersections between a plurality of data signal lines 112 and a plurality of scan signal lines 110 arranged in matrix form. A scan signal line selection circuit 102 supplies a scan signal to the scan signal lines 110 in sequence. The phase-expansion circuit 32 samples an image signal having time-series data corresponding to each of said pixel positions in accordance with a first sampling period, and outputs in parallel a plurality of phase-expaned signals that have been converted to a time length of data that is longer than the first sampling period. A plurality of sampling circuits 106 connected to corresponding data signal lines 112 each receive one of the plurality of phase-expaned signals, samples the pixel data in the phase-expaned signal according to a second sampling period, and supplies a data signal to the data signal lines 112. A sampling signal generation circuit 104 generates a sampling signal having the second sampling period that is shorter than a period of time corresponding to the time length of data in the phase-expaned signals, and supplies it to the sampling circuits 106.

BSPR:
In an active matrix type of liquid crystal display device, for example, an operation of writing data to a liquid crystal layer of each of a number of pixels is implemented by a point-at-a-time scanning, through a switching element that is a thin-film transistor (TFT), where a plurality of these TFTs are connected to a single scan signal line.

BSPR:
However, to answer the recent demands for a device capable of handling multi-media data, such as a personal computer (PC) or engineering workstation (EWS), it is desirable to provide a display having a lot of gray levels such as 256 gray levels when displaying a natural-seeming image such as a video signal.

BSPR:
Unfortunately, it is necessary to sample and hold data from within an image signal in components such as TFT switches, in order to achieve the above point-at-a-time scanning in an active matrix type of liquid crystal display device. This gives rise to a problem in that the switching characteristic of the TFT cannot follow the frequency of the input image signal fast enough. In a display device with an integral driver, the capabilities of sample-and-hold TFTs is lower than in a display device with an external driver, and thus this problem is more obvious. With a high-definition display device having a large number of pixels, the frequency of the input image signal is higher, so this problem is more obvious.

BSPR:

Therefore, a technique has been proposed (in Japanese Patent Application No. 6-316988) whereby the input picture signal is phase-expanded to, for example, six parallel signals as shown in FIG. 32, to increase the time length of data per pixel and reduce the frequency of the signal input to the liquid crystal panel.

BSPR:
This phase expansion makes it possible to increase the time length of data for each pixel and increase the resolution, even with the frequency characteristics of a TFT used as, for example, a sample-and-hold switch.

BSPR:
FIG. 32 shows how the time length of data for each of the phase-expanded signals that are output in parallel after the 6-phase expansion has a time length that is equal to six cycles of a reference clock signal.

BSPR:
When these phase-expanded signals are sampled by the sample-and-hold switch such as a TFT, the sampling period of a sampling signal that is input to the gate of the TFT, for example, is set to eight cycles of the reference clock signal, as shown in FIG. 32, as a test.

BSPR:
This setting is a sufficiently long sampling period with respect to the time length of data in the phase-expande signals, from consideration of the frequency following characteristics of a TFT switch. It also means that a sampling signal having this sampling period can be created easily by using a shift register alone.

BSPR:
Another objective of this invention is to provide an image display device, image display method, and display drive device that make it possible to reduce or prevent ghosting, even when increasing speed of the dot clock signal makes it no longer possible to follow the sample-and-hold operation during the point-at-a-time scanning, as well as electronic equipment that uses that method.

BSPR:
First of all, the present inventor has determined that the cause of ghosting is the intrusion of unwanted components in the waveform supplied through the sampling means to each pixel, as shown in FIG. 34. The intrusion of unwanted components within this waveform is caused by an extension of the second sampling period to eight cycles of the dot clock signal, in comparison with the time length of data in the phase-expanded signal which is six cycles of the dot clock signal, as shown in FIG. 32.

BSPR:
Therefore, taking as an example the video n signal line of FIG. 32, sampling signals S/H(n), S/H(n+6), and S/H(n+12) implement the sampling while there are overlapping periods of time therebetween, so that during the initial sampling period of S/H(n+6), for example, the S/H(n+6) sampling signal samples sampling data while S/H(n) is still sampling.

BSPR:
This invention makes it possible to set the second sampling period of the sampling signal to be always shorter than the time length of data in the phase-expanded signals, as shown in FIGS. 8, 11, 14, and 17, reducing the influences of other data on original data, and thus reducing or preventing ghosting.

BSPR:
With this invention, the phase-expansion means may output the phase-expanded signals in parallel with different head positions of the pixel data in the phase-expanded signals on the basis of a reference clock signal. During this time, the sampling signal generation means may supply the sampling signals to

the plurality of sampling means with different head positions of the second sampling periods in the sampling signals. This ensures that the pixels connected to each of the scan signal lines can be driven by a point-at-a-time scanning.

BSPR:
This shift register has a plurality of stages in which an output signal from each stage is output at a timing that partially overlaps a phase of a preceding-stage output signal. More specifically, the shift register can sequentially shift an input signal, which has a pulse width that is 2N (where N is an integer) times one cycle of the reference clock signal, later than the preceding output signal by one cycle of the reference clock signal. In an example shown in FIG. 7A, N=4 and thus the pulse width of an input signal DX is eight times one cycle of a dot clock signal DC. In another example shown in FIG. 10, N=3 and thus the pulse width of the input signal DX is six times one cycle of the dot clock signal DC. In yet another example shown in FIG. 13, N=2 and thus the pulse width of the input signal DX is four times one cycle of the dot clock signal DC.

BSPR:
Thus the nth and (n+N)th (where: 1.ltoreq.n.ltoreq.(total number of pixels on one scan signal line)) outputs of the shift register are input to the AND circuit connected to the nth sampling means, and the second sampling period for the sampling signal that is the AND thereof is N times one cycle of the reference clock signal.

BSPR:
If, for example, n is assumed to be 1 in an embodiment in which N=4, as shown in FIG. 6, the first and fifth shift register outputs are input to an AND circuit 160a to produce the second sampling period as shown in FIG. 7, which is four (=N) times one cycle of the dot clock signal DC.

BSPR:
If, for example, n is assumed to be 1 in an embodiment in which N=3, as shown in FIG. 9, the first and fourth shift register outputs are input to the AND circuit 160a to produce the second sampling period as shown in FIG. 10, which is three (=N) times one cycle of the dot clock signal DC.

BSPR:
If, for example, n is assumed to be 1 in an embodiment in which N=2, as shown in FIG. 12, the first and third shift register outputs are input to the AND circuit 160a to produce the second sampling period as shown in FIG. 13, which is two (=N) times one cycle of the dot clock signal DC.

BSPR:
The sampling signal generation means may comprise a shift register which outputs a signal later than a preceding signal by one cycle of a reference clock signal. More specifically, the shift register can sequentially shift an input signal, which has a pulse width that is 2N (where N is an integer) times one cycle of the reference clock signal, later than the preceding output signal by one cycle of the reference clock signal.

BSPR:
In the example of FIG. 16, N=4 and thus the pulse width of the input signal DX is eight times one cycle of the dot clock signal DC.

BSPR:
This ensures that, during an mth simultaneous drive {where: 1.ltoreq.m.ltoreq.(total number of pixels on one scan signal line)/(total number of the phase-expanded signal lines)}, the (3m-2)th output of the shift register within one horizontal scanning period of time can be input to the plurality of sampling means, and the second sampling period of the sampling means can be N times one cycle of the reference clock signal.

BSPR:

The write capabilities of a TFT are limited, but the sufficiently long second sampling period can be ensured by inputting phase-expanded signals having pixel. data with a long time length of data, and, since previous pixel data is not written during the second sampling period, the intrusion of unwanted components into the waveform can be reduced, making it possible to effectively prevent ghosting.

BSPR:
In such a case, the image display device may comprise polarity inversion means in a stage before the phase-expansion means, for receiving the image signals, generating a first-polarity image signal which drives the pixels at a first polarity with respect to a polarity inversion reference potential and a second-polarity image signal which drives the pixels at a second polarity that is the opposite of the first polarity, and outputting one of the first- and second-polarity image signals to the phase-expansion means. During this time, the phase-expansion means performs phase expansion for the first- and second-polarity image signals and outputs first- and second-polarity phase-expanded signals.

BSPV:
phase-expansion means for sampling image signals each of which has time-series data corresponding to each of the pixel positions in accordance with a first sampling period, converting the image signals into a plurality of phase-expansion signals to have a plurality of pixel data, respectively, and outputting the phase-expanded signals in parallel, and a length of each of the pixel data being longer than the first sampling period for the image signals;

BSPV:
a plurality of sampling means connected to the data signal lines, respectively, each of the plurality of sampling means receiving one of the phase-expanded signals, sampling the plurality of pixel data in a received phase-expanded signal in accordance with sampling signals having second sampling periods, and supplying sampled pixel data as a data signal to one of the data signal lines; and

BSPV:
sampling signal generation means for generating the sampling signals which have the second sampling periods which are each shorter than a period of time corresponding to a time length of each of the pixel data in the phase-expanded signals, and for supplying the sampling signals to the plurality of sampling means.

DRPR:
FIG. 8 is a characteristic diagram showing the relationship between the time length of data in the phase-expanded signals of the first embodiment and the sampling period;

DRPR:
FIG. 11 is a characteristic diagram showing the relationship between the time length of data in the phase-expanded signals of the second embodiment and the sampling period;

DRPR:
FIG. 14 is a characteristic diagram showing the relationship between the time length of data in the phase-expanded signals of the third embodiment and the sampling period;

DRPR:
FIG. 17 is a characteristic diagram showing the relationship between the time length of data in the phase-expanded signals of the fourth embodiment and the sampling period;

DEPR:
The timing generation circuit block 20 receives a clock signal CLK and a synchronization signal SYNC, and outputs a predetermined timing signal.

DEPR:
On the liquid crystal panel 100 are formed a plurality of scan signal lines 110 which extend in the row direction by way of example in FIG. 1 and a plurality of data signal lines 112 which extend in the column direction by way of example in FIG. 1. Note that, in this embodiment, the total number of scan signal lines 110 is 492 and the total number of data signal lines 112 is 652. A display element consisting of a switching element 114 and a liquid crystal layer 116 connected in series is; constructed at each pixel position created by the intersection of the lines 110 and 112, to form a pixel. A period of time during which the switching element 114 is. on is called a selected period and a period of time during which it is off is called a non-selected period. A holding capacitor (not shown in the figure) which holds in the non-selected period a voltage that is supplied during the selected period to the liquid crystal layer 116 through the switching element 114 is connected to the liquid crystal layer 116. In this embodiment, the switching element 114 could be configured of a 3-terminal type of switching element such as a TFT. Note, however, that it is not limited thereto; a 2-terminal type of switching element such as a metal-insulator-metal (MIM) element or metal-insulator-semiconductor (MIS) element could be used therefor. Note that the liquid crystal panel 100 of this embodiment is not limited to an active matrix type of liquid crystal display device using 2-terminal or 3-terminal switching; it can equally well be another type of liquid crystal panel such as a passive matrix type of liquid crystal display panel. The liquid crystal panel 100 of this embodiment has a first substrate on which are formed the scan signal lines 110 and the data signal lines 112, together with the TFTs connecting these lines. In this first substrate are also formed pixel electrodes connected to the TFTs and holding capacitors that use each of the pixel electrodes as an electrode on one side. The liquid crystal panel 100 also has a second substrate which is disposed facing the first substrate and on which is formed a common electrode. A liquid crystal is inserted between the first and second substrates to form the liquid crystal panel 100. One side of a liquid crystal layer at each pixel position acts as a pixel electrode and another side acts as a common electrode, and an electric field is applied to the liquid crystal layer by these two electrodes.

DEPR:
The scan-side drive circuit 102 outputs to a plurality of scan signal lines 110a, 110b, etc., a scan signal in which a selected period has been set, to sequentially select the scan signal line 110.

DEPR:
The data-side drive circuit 104 outputs a sampling signal to sample-and-hold switches 106 disposed between the six phase-expanded signal lines Data1 to Data 6, which are the output lines of the data processing circuit block 30, and the data signal lines 112a, 112b, etc., of the liquid crystal panel 100, for driving the liquid crystal panel 100 by the point-at-a-time scanning.

DEPR:
As shown in FIG. 2, the image signal that is input to the data processing circuit block 30 is an analog signal having time-series data corresponding to each pixel in the liquid crystal panel 100. The phase-expansion circuit 32 that performs the 6-phase expansion samples this image signal in accordance with a reference clock signal such as a dot clock signal DC which has a first sampling period. It then generates six phase-expanded signals that have been converted to have a data length that is longer than the sampling period with which this image signal was sampled. In this embodiment, the data is extended to a length that is an integral multiple of one cycle of the dot clock signal DC, to give six parallel phase-expanded signals. This means that the phase-expansion circuit 32 has a function for extending the data length and a function for converting the serial image signal into parallel image signals. With the first phase-expanded signal that is output on the first phase-expanded signal line Data1, for example, data for the first, seventh, and thirteenth pixels of the picture signal is extended to a time length of data that is six times one cycle of the dot clock signal DC. Similarly, the

data for every sixth pixel onward is extended to that time length of data.

DEPR:
Note that each of the first to sixth phase-expanded signals that are output on the first to sixth phase-developed signal lines Data1 to Data6 is output in a state such that the head position of each set of pixel data is sequentially shifted by one cycle of the dot clock signal DC from the preceding phase-expanded signal.

DEPR:
Specific examples of the 6-phase expansion circuit and polarity inversion circuit are shown in FIGS. 3, 4A, and 4B. In FIG. 3, the phase-expanded circuit 32 is configured of switches 500a to 500f, capacitors 502a to 502f, and buffers 504a to 504f. Sampling clock signals SCLK1 to SCLK6 of phases that are different as shown for example in FIG. 5 are each input to the switches 500a to 500f in a one-to-one relationship. Each of these switches 500a to 500f samples data when turned on by the corresponding clock signal, to charge data voltage in the corresponding subsequent-stage capacitors 502a to 502f. Each of these switches 500a to 500f holds a data potential while it is turned off by the corresponding clock signal. This provides the six phase-expanded signals through the buffers 504a to 504f, as shown in FIG. 5.

DEPR:
In the example shown in FIG. 3, six amplifier circuits 506a to 506f and six polarity inversion circuits 508a to 508f are necessary since the amplification and polarity inversion are implemented after the phase expansion. However, since the capacitors 502a to 502f can store the signal charge at a stage before the signal is amplified, when the signal amplitude is small, the time required for charging is small, so this method is advantageous in that it can be made faster.

DEPR:
This data-side drive circuit 104 has shift registers 120, 130, 140 and 150 for first to fourth columns, as shown in FIG. 6. The shift registers 120 to 150 each receive an input signal DX that forms common shift data, as shown in FIG. 7A. This input signal DX is high for eight cycles of the dot clock signal DC, as shown in FIG. 7A. A first clock signal CLX1 and a first inverted clock signal thereof are input to the shift register 120 of the first system, as shown in FIG. 6. As the first clock signal CLX1, a pulse of half the width of the input signal DX is output repeatedly at a cycle that is the pulse width of the input signal DX, as shown in FIG. 7A. In a similar manner, second to fourth clock signals CLX2 to CLX4 and inverted clock signals thereof are input to the shift registers 130 to 150 of the second to fourth systems. Each of the second to fourth clock signals CLX2 to CLX4 rises later than the preceding clock signal by one cycle of the dot clock signal DC.

DEPR:
The shift registers 120 to 150 of each system are each configured to comprise a multi-stage master/slave type of clocked inverter. Concentrating on a description of the first stage of the first shift register 120, a first clocked inverter 121a that acts as master is connected in series with an inverter 121b, and a second clocked inverter 121c that acts as slave is connected to a feedback line that connects the input and output lines of the inverter 121b. The master clocked inverter 121a inverts and outputs the input signal DX when the first clock signal CLX1 is high. Similarly, the second, slave clocked inverter 121c inverts and outputs an output signal of the inverter 121b when the first inverted clock signal /CLX1 is high.

DEPR:
During the first half portion that the input signal DX is high (for four cycles of the dot clock signal DC), the first clock signal CLX1 is high and the input signal DX is inverted to low and is output as the output of the first clocked inverter 121a. This low-level signal is inverted by the inverter 121b. Therefore, as the output of the first stage of the first system shift register 120, only the first half portion of the input signal DX is output

high as indicated by SR1-OUT1 in FIG. 7A.

DEPR:
During the second half portion of the input clock signal DX, the clock signal CLX1 is low but contrary the first inverted clock signal /CLX1 that is input to the second, slave clocked inverter 121c is high. The signal input to this second clocked inverter 121c is a high-level signal from the inverter 121b so that, as a result, the output from the second clocked inverter 121c is the inversion of this input high-level signal and is thus a low-level signal. This low-level signal is inverted by the inverter 121b. Therefore, the second half portion of the first output signal SR1-OUT1, which is the output of the first stage of the first-system shift register 120, is also output as a high-level signal.

DEPR:
Each of the second to fourth output signals SR2-OUT1 to SR4-OUT1 is output later than the preceding output signal by one cycle of the dot clock signal DC, by the operations of the first stages of each of the shift registers 130 to 150 of the second to fourth systems, as shown in FIG. 7A.

DEPR:
The first output signal SR1-OUT1 that is output from the first stage of the first-system shift register 120 and the fifth output signal SR1-OUT2 that is output from the second stage thereof are input to the NAND circuit 160a provided in the stage before the sample-and-hold switch 106a that is connected to the first data signal line 112a. Therefore, a sampling signal SL1-Data1 obtained through this NAND circuit 160a and the inverter 162a in the next stage is an AND of the first output signal SR1-OUT1 and the fifth output signal SR1-OUT2, as shown in FIG. 7A, and a period of time that is four cycles of the dot clock signal DC is set to be the second sampling period.

DEPR:
The signal SR2-OUT1 from the first stage of the second-system shift register 130 and the signal SR2-OUT2 from the second stage thereof are input to the NAND circuit 160b in the stage before the sample-and-hold switch 106b that is connected to the second data signal line 112b. Therefore, a second sampling signal SL2-Data2 obtained through this NAND circuit 160b and the inverter 162b of the next stage is delayed by one cycle of the dot clock signal DC after the first sampling signal SL1-Data1, but the sampling period thereof is the same four cycles of the dot clock signal DC. Note that the operation is the same for each data signal line from the third data signal line onward.

DEPR:
The relationship between the phase-expanded signals Data1 to Data6 that are input to the sample-and-hold switches 106 and the sampling signals SL(n)-Data(m) is shown in FIG. 8. In FIG. 8, sampling signals SL1-Data1, SL7-Data1, and SL13-Data1 that sample the phase-expanded signal Data1 are shown. Information in the first sample-and-hold switch 106a and having a data length that is six cycles of the dot clock signal DC, as shown in FIG. 8, is input to the source line of the TFT configuring the sample-and-hold switch 106a. Similarly, the sampling signal SL1-Data1 is input through the NAND circuit 160a and the inverter 162a to the gate of the TFT configuring the sample-and-hold switch 106a. The sampling signal SL1-Data1 is set to a sampling period (time during which it is high) of four cycles of the dot clock signal, which is one cycle less at beginning and end than the six cycles of the time length of data in the phase-expanded signal.

DEPR:
Setting the sampling period in this manner makes it possible to provide a liquid crystal display wherein the previous data does not affect the display, even if the sample-and-hold switches 106 are configured of TFTs and have the limits of the write capabilities of TFTs. In other words, a liquid crystal display with no ghosting can be provided.

DEPR:

That is because the gates of the TFTs configuring the sample-and-hold switches 106 are opened by the sampling signal going high, after the image data on each phase-expanded signal line has stabilized. Moreover, the gates of the TFTs are closed before the data on these phase-expanded signal lines has changed. Since the sample-and-hold switches 106a, 106g, 106n, etc., connected to the same phase-expanded signal line Data1 are driven in such a manner that there is no overlapping period of time during which SL1-Data1, SL7-Data1, SL13-Data1, etc., are high, there is no point at which a plurality of gates are open simultaneously. Therefore, setting the sampling period to be in a stabilized data region within the data length of the phase-expanded signal ensures that only stabilized data, which is not affected by the previous data, is sent out over the data signal lines 112. This data is written to each liquid crystal layer 116 and holding capacitor through the corresponding switching element 114 that is turned on by the scan signal from the scan-side drive circuit 102.

DEPR:
In a similar manner, stabilized data is thereafter sent through the sampling switches 106b, 106c, etc., to the sequentially corresponding data signal lines 112b, 112c, etc., to implement write by point-at-a-time scanning to each liquid crystal layer 116 connected to the first scan signal line 110a through the switching elements 114. This data write is subsequently repeated while the switching elements 114 connected to the scan signal lines 110 from the second scan signal line onward are sequentially switched on by the scan signal from the scan-side drive circuit 102.

DEPR:
This second embodiment implements a liquid crystal display drive by using phase-expanded signals having a data length that is six cycles of the dot clock signal and a sampling signal having a sampling period that is three cycles of the dot clock signal.

DEPR:
The data-side drive circuit 104 shown in FIG. 9 has shift registers 200, 210 and 220 of the first to third systems. These shift registers 200 to 220 receive the input signal DX which is common shift data, as shown in FIG. 10. This input signal DX is high over six cycles of the dot clock signal DC, as shown in FIG. 10. The first-system shift register 200 receives a first clock signal CLK1 and a first inverted clock signal /CKL1 thereof, as shown in FIG. 10. As the first clock signal CLK1, a pulse of half the pulse width of the input signal DX is output repeatedly at a cycle that is the same as the pulse width of the input signal DX, as shown in FIG. 10. In a similar manner, the second- and third-system shift registers 210 and 220 each receive second and third clock signals CLK2 and CLK3 and inverted clock signals /CLK2 and /CLK3 thereof. Each of the second and third clock signals CLK2 and CLK3 rises later than the preceding clock signal by one cycle of the dot clock signal DC.

DEPR:
The first output signal SR1-OUT1 from the first stage of the first-system shift register 200 and the fourth output signal SR1-OUT2 from the second stage thereof are input to the NAND circuit 160a provided in the stage before the sample-and-hold switch 106a that is connected to the first data signal line 112a. Therefore, a sampling signal SL1-Data1 obtained through this NAND circuit 160a and the inverter 162a in the next stage is an AND of the first output signal SR1-OUT1 and the fourth output signal SR4-OUT2, and a period of time that is high for three cycles of the dot clock signal DC is set to be the sampling period, as shown in FIG. 10.

DEPR:
In a similar manner, the signal SR2-OUT1 from the first stage of the second-system shift register 210 and the signal SR2-OUT2 from the second stage thereof are input to the NAND circuit 160b in the stage before the sample-and-hold switch 106b that is connected to the second data signal line 112b. Therefore, a second sampling signal SL2-Data2 obtained through this NAND circuit 160b and the inverter 162b of the next stage is delayed by one cycle

of the dot clock signal DC after the first sampling signal SL1-Data1, but the sampling period thereof is high for the same three cycles of the dot clock signal DC. Note that the operation is the same for each data signal line from the third data signal line onward.

DEPR:
It should be noted that a seventh sampling signal SL7-Data1 shown in FIG. 10 samples the same phase-expanded signal line Data1 as the first sampling signal SL1-Data1 does. As is clear from FIG. 10, these two sampling periods are not overlapping.

DEPR:
The relationship between the phase-expanded signals Data1 to Data6 that are input to sampling switches 102 and the sampling signals SL(n)-Data(m) is shown in FIG. 11. This FIG. 11 shows the same waveforms as those of FIG. 8. For example, information having a time length of data that is six cycles of the dot clock signal DC, as shown in FIG. 11, is input to the source line of the TFT configuring the sample-and-hold switch 106a. Similarly, the sampling signal SL1-Data1 is input through the NAND circuit 160a and the inverter 162a to the gate of the TFT configuring the sample-and-hold switch 106a. This sampling signal SL1-Data1 is set to have a sampling period of three cycles of the dot clock signal, which is 1.5 cycles less at beginning and end than the six cycles of the dot clock signal which correspond to the data length of the phase-expanded signal, as shown in FIG. 11. Thus stabilized data that is not affected by previous data can be written, in the same manner as in the first embodiment.

DEPR:
This third embodiment implements a liquid crystal display drive by using phase-expanded signals having a data length that is six cycles of the dot clock signal and a sampling signal having a sampling period that is two cycles of the dot clock signal.

DEPR:
The data-side drive circuit 104 shown in FIG. 12 has shift registers 300 and 310 of the first and second systems. These shift registers 300 and 310 receive the input signal DX which is common shift data that is high over four cycles of the dot clock signal DC, as shown in FIG. 13. The first-system shift register 300 receives a first clock signal CLK1 and a first inverted clock signal /CKL1 thereof, as shown in FIG. 12. As the first clock signal CLK1, a pulse of half the pulse width of the input signal DX is output repeatedly at a cycle that is the same as the pulse width of the input signal DX, as shown in FIG. 13. In a similar manner, the second-system shift register 310 receives a second clock signal CLK2 and an inverted clock signal thereof. The second clock signal CLK2 rises later than the first clock signal CLK1 by one cycle of the dot clock signal DC.

DEPR:
The first output signal SR1-OUT1 from the first stage of the first-system shift register 300 and the third output signal SR1-OUT2 from the second stage thereof are input to the NAND circuit 160a provided in the stage before the sample-and-hold switch 106a that is connected to the first data signal line 112a. Therefore, a sampling signal SL1-Data1 obtained through this NAND circuit 160a and the inverter 162a in the next stage is an AND of the first output signal SR1-OUT1 and the third output signal SR1-OUT2, as shown in FIG. 13, and a period of time that is two cycles of the dot clock signal DC is set to be the sampling period.

DEPR:
In a similar manner, the signal SR2-OUT1 from the first stage of the second-column shift register 310 and the signal SR2-OUT2 from the second stage thereof are input to the NAND circuit 160b in the stage before the sample-and-hold switch 106b that is connected to the second data signal line 112b. Therefore, a second sampling signal SL2-Data2 obtained through this NAND circuit 160b and the inverter 162b of the next stage is delayed by one cycle

of the dot clock signal DC after the first sampling signal SL1-Data1, but the sampling period thereof is the same two cycles of the dot clock signal DC. Note that the operation is the same for each data signal line from the third data signal line onward.

DEPR:
The relationship between the phase-expanded signals Data1 to Data6 that are input to the sampling switches 102 and the sampling signals SL(n)-Data(m) is shown in FIG. 14. This FIG. 14 shows the same waveforms as those of FIG. 8. For example, information having a time length of data that is six cycles of the dot clock signal DC, as shown in this figure, is input to the source line of the TFT configuring the sample-and-hold switch 106a. Similarly, the sampling signal SL1-Data1 is input through the NAND circuit 160a and the inverter 162a to the gate of the TFT configuring the sample-and-hold switch 106a. This sampling signal SL1-Data1 is set to have a sampling period of two cycles of the dot clock signal, which is two cycles less at beginning and end than the six cycles of the dot clock signal which correspond to the time length of data in the phase-expanded signal. Thus stabilized data that is not affected by previous data can be written, in the same manner as in the first and second embodiments.

DEPR:
This fourth embodiment modifies the point-at-a-time scanning of the first and third embodiments to provide simultaneous driving of the same number of pixels as the number of expansion phases, such as 6-pixel simultaneous drive. With an engineering workstation (EWS) for instance, the frequency of the dot clock signal is increased (to 130 MHz, for example) and the phase difference for point-at-a-time scanning is no more than 10 ns. If the sample-and-hold switches are TFTs in such a case, the switching cannot possibly follow the increased frequency. It is therefore efficient to drive a plurality of pixels simultaneously in such a case. This fourth embodiment will be described below with reference to FIGS. 15 to 17.

DEPR:
Therefore, a data processing circuit block 30 of this fourth embodiment, shown in FIG. 15, is also provided with a sample-and-hold circuit 36 between the phase-expansion circuit 32 and the amplification and inversion circuit 34. A first sample-and-hold operation of the phase-expansion circuit 32 shifts each of the head positions of the pixel data of the phase-expanded signals by one cycle of the dot clock signal DC from the preceding phase-expanded signal, as shown in FIG. 2. However, these are again sampled and held together in the sample-and-hold circuit 36 of the next stage, so that the head positions of the pixel data are aligned in the first to sixth phase-expanded signals output over the first to sixth phase-expanded signal lines Data1 to Data6, as shown in FIG. 17. Note that buffer memory could be used as the sample-and-hold circuit 36 of the next stage. Furthermore, the amplification and inversion circuit 34 could be disposed in the stage before the phase-expansion circuit 32.

DEPR:
As shown in FIG. 15, the data-side drive circuit 104 has a first-system shift register 400. The input signal DX, the clock signal CLK, and the inverted clock signal thereof that are shift data input to the shift register 400, are the same as the input signal DX, the first clock signal CLX, and the inverted clock signal of the first embodiment that are shown in FIG. 7. In other words, the input signal DX is high for eight cycles of the dot clock signal DC, as shown in FIG. 16. As the clock signal CLK, a pulse of half the width of the input signal DX is output repeatedly at a cycle that is the pulse width of the input signal DX, as shown in FIG. 16.

DEPR:
As a result, a period of time that is four cycles of the dot clock signal DC is set in common as a sampling period, with respect to a phase-expanded signal of a data length that is six cycles of the dot clock signal DC, as shown in FIG. 17. Thus stabilized data that is not affected by previous data can be

written, in the same manner as in the first to third embodiments.

DEPR:
Note that the same input signal DX, clock signal CLX, and inverted clock signal thereof as those of the first embodiment are used by this fourth embodiment, but signals corresponding to those of the second and third embodiments can also be used. If the signals of the second embodiment are used, a period of time that is three cycles of the dot clock signal DC is set in common as the sampling period. Similarly, if the signals of the third embodiment are used, a period of time that is two cycles of the dot clock signal DC is set in common as the sampling period.

DEPR:
A timing chart of the operation of the circuit of FIG. 19 is shown in FIG. 20. The outputs of the phase-expansion circuit 32 of FIG. 19 correspond to the first sample-and-hold outputs of FIG. 20 and equal to the six phase-expanded signals as described above. Switches 550a to 550f provided in the sample-and-hold circuit 36 of FIG. 19 are simultaneously driven on and off on the basis of a sampling clock signal SCLK7 of FIG. 20. As a result, the head positions of pixel data in the outputs of buffers 554a to 554f of FIG. 19 are aligned, as shown by the second sample-and-hold outputs in FIG. 20.

DEPR:
This seventh embodiment is a variant of FIG. 19, wherein two sample-and-hold circuits 36 and 38 are provided in a stage after the phase-expansion circuit 32, as shown in FIG. 21. A timing chart illustrating the operation of the circuit of FIG. 21 is shown in FIG. 22. The outputs of the phase-expansion circuit 32 of FIG. 21 correspond to the first sample-and-hold outputs of FIG. 22 and equal to the six phase-expanded signals. Switches 550a to 550c provided in the sample-and-hold circuit 36 of FIG. 21 are simultaneously driven on and off on the basis of a sampling clock signal SCLK7 of FIG. 22. As a result, the head positions of pixel data in the outputs of buffers 554a to 554c of FIG. 21 are aligned, as shown by the second sample-and-hold outputs in FIG. 22. Switches 550d to 550f provided in the sample-and-hold circuit 36 of FIG. 21 are simultaneously driven on and off on the basis of a sampling clock signal SCLK8 of FIG. 22. As a result, the head positions of pixel data in the outputs of buffers 554a to 554c of FIG. 21 are aligned, as shown by the second sample-and-hold outputs in FIG. 22. Switches 560a to 560f provided in the final-stage sample-and-hold circuit 38 of FIG. 21 are simultaneously driven on and off on the basis of a sampling clock signal SCLK9 of FIG. 22. As a result, the head positions of pixel data in the outputs of buffers 564a to 564f of FIG. 21 are aligned, as shown by the third sample-and-hold outputs in FIG. 22.

DEPR:
In this manner, each set of data sampling can always be done with respect to the data regions in the six phase-expanded time lengths except for the edges of the data region. This prevents unwanted components from intruding into the waveforms supplied to the display elements of the liquid crystal panel, improving quality.

DEPR:
Six different sampling clock signals SHCL1 to SHCL6 are provided for driving the first to sixth switches 500a to 500f, as shown in FIG. 24, and these are generated by a timing generation circuit block 20 on the basis of select signals Si to S6. With this device, the six different sampling clock signals SHCL1 to SHCL6 are supplied by selectively switching the select signals S1 to S6, on the basis of the horizontal and vertical synchronization signals for driving the liquid crystal panel 10. For this purpose, a six-digit counter for counting the horizontal synchronization signal is provided within the timing generation circuit block 20. Every time the six-digit counter increments, in other words, every time another of the scan signal lines 110 of FIG. 1 is selected for a horizontal scan (1H), the select signals S1 to S6 are switched sequentially for output.

DEPR:
Electronic equipment that uses an image display device in accordance with one of the above described embodiments comprises a display information output source 1000, a display information processing circuit 1002, a display drive circuit 1004, a display panel 1006 such as a liquid crystal panel, a clock signal generation circuit. 1008, and a power circuit 1010, as shown in FIG. 27. The display information output source 1000 comprises memory such as ROM and RAM, and tuning circuitry for tuning and outputting a television signal, and outputs display information such as a video signal on the basis of a clock signal from the clock signal generation circuit 1008 that corresponds to the above described timing generation circuit block 20. The display information processing circuit 1002 corresponds to the data processing circuit block 30 of the above embodiments, and processes and outputs display information on the basis of the clock signal from the clock signal generation circuit 1008. In addition to the above described amplification and polarity inversion circuits, phase-expansion circuits, and rotation circuits, etc., this display information processing circuit 1002 could also comprise components such as a gamma correction circuit and clamp circuit that are known in the art. The display drive circuit 1004 comprises the above described scan-side drive circuit 102 and data-side drive circuit 104, to drive the liquid crystal panel 1006. The power circuit 1010 supplies power to all of the above circuits.

DEPR:
It should be noted that the present invention is not limited to the above described embodiments and it can be modified in many various ways within the range of the invention. For example, this invention is not limited to the driving of various liquid crystal display devices as described above; it can equally well be applied to image display devices that use electroluminescence, plasma display devices, or CRTs. Similarly, the number of phase expansions, the time length of data in the phase-expanded signals, and the corresponding length of the sampling period can be modified in various ways in addition to those described in the above embodiments.

CLPV:
a phase-expansion circuit that samples an image signal which has time-series data corresponding to each of said pixel positions in accordance with a first sampling period, converting said image signal into a plurality of phase-expanded signals including a plurality of pixel data, respectively, and outputting said phase-expanded signals in parallel, and a time-length of each of said pixel data being longer than said first sampling period;

CLPV:
a plurality of sampling circuits connected to said data signal lines, respectively, each of said plurality of sampling circuits receiving one of said phase-expanded signals, samples said plurality of pixel data in a received phase-expanded signal in accordance with sampling signals having second sampling periods, and supplies sampled pixel data as a data signal to one of said data signal lines; and

CLPV:
a sampling signal generator that generates said sampling signals which have said second sampling periods that are each shorter than a period corresponding to a time length of each of said pixel data in said phase-expanded signals, and that supplies said sampling signals to said plurality of sampling circuits.

CLPV:
wherein said phase-expansion circuit outputs said phase-expanded signals in parallel with different head positions of said pixel data in said phase-expanded signals on the basis of a reference clock signal;

CLPV:
wherein said sampling signal generator supplies said sampling signals to said plurality of sampling circuits with different head positions of said second sampling periods of said sampling signals; and

CLPV:
wherein said pixels connected to each of said scan signal lines are driven by a point-at-a-time scanning.

CLPV:
wherein said sampling signal generator comprises a shift register which outputs a signal later than a preceding signal by one cycle of a reference clock signal;

CLPV:
wherein during an mth simultaneous drive {(where: 1.ltoreq.m.ltoreq.(total number of pixels on one scan signal line)/(total number of said phase-expanded signal lines)}, the (3m-2)th output of said shift register during one horizontal scanning period is input to said plurality of sampling circuits.

CLPV:
a phase-expansion circuit that samples an image signal which has a time-series data corresponding to each of said pixel positions in accordance with a first sampling period, converts said image signal into a plurality of phase-expanded signals including a plurality of pixel data, respectively, and outputs said phase-expanded signals in parallel, and a time length of each of said pixel data being longer than said first sampling period;

CLPV:
a plurality of sampling circuits connected to said data signal lines, respectively, each of said plurality of sampling circuits receives one of said phase-expanded signals, samples said plurality of pixel data in a received phase-expanded signal in accordance with sampling signals having second sampling periods, and supplies sampled pixel data as a data signal to one of said data signal lines; and

CLPV:
a sampling signal generator that generates said sampling signals which have said second sampling periods that are each shorter than a period corresponding to a time-length of each of said pixel data in said phase-expanded signals, and that supplies said sampling signals to said plurality of sampling circuits.

CLPV:
a step of sampling an image signal which has a time-series data corresponding to each of said pixel positions in accordance with a first sampling period, converting said image signal into a plurality of phase-expanded signals having a plurality of pixel data, respectively, and outputting said phase-expanded signals in parallel, and a time length of each of said pixel data being longer than said first sampling period;

CLPV:
a step of sampling said plurality of pixel data in each of said phase-expanded signals in accordance with second sampling periods that are each shorter than a period corresponding to a time length of each of said pixel data in said phase-expanded signals; and

CLPV:
phase-expansion means for sampling an image signal which has time-series data corresponding to each of said pixel positions in accordance with a first sampling period, converting said image signal into a plurality of phase-expanded signals including a plurality of pixel data, respectively, and outputting said phase-expanded signals in parallel, and a time-length of each of said pixel data being longer than said first sampling period;

CLPV:
a plurality of sampling means connected to said data signal lines, respectively, each of said plurality of sampling means receiving one of said phase-expanded signals, sampling said plurality of pixel data in a received

phase-expanded signal in accordance with sampling signals having second sampling periods, and supplying sampled pixel data as a data signal to one of said data signal lines; and

CLPV:
sampling signal generation means for generating said sampling signals which have said second sampling periods that are each shorter than a period corresponding to a time length of each of said pixel data in said phase-expanded signals, and for supplying said sampling signals to said plurality of sampling means.

CLPV:
phase-expansion means for sampling an image signal which has a time-series data corresponding to each of said pixel positions in accordance with a first sampling period, converting said image signal into a plurality of phase-expanded signals including a plurality of pixel data, respectively, and outputting said phase-expanded signals in parallel, and a time length of each of said pixel data being longer than said first sampling period;

CLPV:
a plurality of sampling means connected to said data signal lines, respectively, each of said plurality of sampling means receiving one of said phase-expanded signals, sampling said plurality of pixel data in a received phase-expanded signal in accordance with sampling signals having second sampling periods, and supplying sampled pixel data as a data signal to one of said data signal lines; and

CLPV:
sampling signal generation means for generating said sampling signals which have said second sampling periods that are each shorter than a period corresponding to a time-length of each of said pixel data in said phase-expanded signals, and for supplying said sampling signals to said plurality of sampling means.